REMARKS

Currently pending in the application are claims 1-33, of which claims 1, 16 and 19-27 are independent. Applicants thank the Examiner for the indication that claims 13 and 14 are in condition for allowance if rewritten in independent form.

Claim Objections:

In regards to the Examiner's objection to pending claim 18, wherein the phrase "allocating a counter variable that is not otherwise specified in the description of the finite state machine model" is deemed unclear, Applicants respectfully submit that said phrase is clear in view of paragraph [0011] of the pending specification. As recited in paragraph [0011), prior art systems and solutions have used *a counter variable associated with a finite state machine,* which is specified in the description of the finite state machine model, in conjunction with explicit action statements to test the counter variable upon execution of an event. In contrast, the phrase of claim 18 recites the allocation of a counter variable *that is not specified in the description of the finite state machine model* for use in emulating the described finite state machine model. In view of this distinction, Applicants respectfully submit that cited phrase is clear and concise as presented. Applicants therefore request that the Examiner withdraw the objection to claim 18.

Claim Rejections under 35 USC § 102

The Examiner states that claims 1-12, 15-33 are unpatentable over Jones et al. (US patent No. 5,956,741). Applicant respectfully traverses this rejection on the basis that the cited art to Jones fails to recite each element of the present invention. In particular, Applicants submit that the Jones reference fails to recite the receiving of a finite state machine model, a temporal logic operator and the step of generating code for emulating the finite state machine model.

Claim 1 recites a method for operating a computer system. In the method, a description of a finite state machine model is received in the system wherein the description

includes a temporal logic operator for defining a temporal logic condition. A temporal logic operator is a Boolean function that may be used in a conditional expression associated with a state. A temporal logic operator has at least one parameter: an event E. The operator may also have others parameters, such as a threshold value. The value of the temporal logic operator at a given time is determined by the number occurrences of event E during the current activation of the state with which it is associated. Examples of temporal logic operators for use with a preferred embodiment of this invention there are four temporal logic operators: after(T, E), before(T, E), at(T, E), and every(T, E). In each case, the parameter E is an event defined in the state diagram, and the parameter T is a numerical expression representing a threshold value. The after operator is defined to be true if and only if event E has occurred at least T times during the current activation of state A. The before operator is defined to be true if and only if event E has occurred less than T times during the current activation of state A. The at operator is defined to be true if and only if event E has occurred exactly T times during the current activation of state A. The every operator is defined to be true at every Tth occurrence of event E during the current activation of state A. One example language capable of use with the present invention is the Stateflow(r) programming language, as offered by the MathWorks of Natick, Massachusetts.

Claim 1 also includes an element capable of generating code for emulating the described finite state machine model. Dependent claims 2-12 and 15 , which rely on independent claim 1 for support, serve to further clarify and limit that which is claimed in independent claim 1. Independent claims 16, 19-24 further recite various methods, system and software component claims that recite similar limitations.

Independent claims 25 and 26 further recite a computer programming system and method comprising the use of a central processing unit, a mass storage subsystem, a program editor for use in including a temporal logic operator for defining a temporal logic condition and a code generator or emulator for generating emulation code, or emulating directly, a finite state machine model. Furthermore, independent claim 27 recites the modeling of a system in a model environment by building a graphical representation of the system and using a temporal logic operator for defining a temporal logic condition for operating the system on temporal logic. Dependent claims 28-33 further clarify and limit that which is recited in independent claim 27.

In contrast, the cited reference to Jones et al. is directed to configurable RAM interface which connects a computer bus to a block of RAM. This RAM interface is adapted to receive, at a high data arrival rate, large multiword variable length tokens by using a swing buffer and a buffer manager. Associated with the buffer manager is a state machine which transitions among a plurality of states, maintaining status information about the buffers, allocating the buffers for reference by a write address generator, clearing the buffers for occupation by subsequently arriving data, and maintaining status information concerning the buffers. The buffer manager also examines tokens of received data in order to update the status of the arrival buffer. The preferred embodiments of Jones are directed to the display of images on a computer system, wherein these images are in the H.261, JPEG and MPEG formats.

In rejecting claim 1, the Examiner states that Jones reference recites each element of the pending claim. Applicants respectfully traverse this rejection. Applicants submit that the cited Figures 1 and 24 of Jones fail to recite or disclose the *receiving of a finite state machine model*, the existence of a *temporal logic operator* and the *generating of code for emulating the finite state machine model.*

As recited in the present invention, a finite state machine model is described in terms of "states," "transitions," and "events", wherein one or more of the states of the machine is said to be "active." The finite state machine model of the present invention comprising at least two state definitions and at least one definition of a transition between the states. This finite state machine model includes a description of said model which is *received* by the computer system.

In contrast, the "finite state machine" of the Jones art, serves to:

> "coordinate the operation of the other blocks. In response to data, the parser state machine controls the other blocks by generating a control word which is passed to the other blocks, side by side with the data upon which this control word acts. Passing the control word alongside the associated data is not only useful, it is essential, since these blocks are connected via a two-wire interface.... Among other things, this code word identifies the particular standard that is being decoded." (column 37, lines 50-61)

In view of such language, Applicants submit that the "parser state machine" of Jones firstly fails to recite or disclose the element of receiving a description of a finite state machine model by a computer system. Additionally, Applicants respectfully submit that the "parser state machine" further fails to trigger actions or states based on events, as recited by the finite state machine model of the present invention, and therefore does not anticipate the finite state machine element of the present invention.

Regarding the temporal logic operator of the present invention, Applicants further submit that this element is not recited by the cited art to Jones. As defined in paragraph [0035] of the present invention,

> "A temporal logic operator is a type of Boolean function that may be used in a conditional expression associated with a state (including a transition leading from the state). A temporal logic operator has at least one parameter: an event E. The operator may also have others parameters, such as a threshold value. The value of the temporal logic operator at a given time is determined by the number occurrences of event E during the current activation of the state with which it is associated"

In contrast, the "temporal logic operator" of Jones, is a Huffman decoder, represented by hardware, used in the display of images. The temporal decoder of Jones reduces the redundancy between a first subject picture and a second picture which arrives prior to the arrival of the subject picture, as well as a third picture which arrives after the arrival of the subject picture. The temporal decoder of Jones further provides a link to an alternative network for addressing these first, second and third pictures using the smallest number of circuits necessary, thereby increasing speed and accuracy in the display of a picture. This link is not the operator, such as an after, before, at, or every operator, as recited in the present invention.

In view of this, Applicants respectfully submit that the Jones Art fails to recite or disclose the temporal logic operator of the present invention.

Regarding the generation of code for emulating the described finite state machine model, Applicants further submit that the Jones reference fails to anticipate the present invention in

view of the fact that the "finite state machine" (i.e. parser state machine) of Jones, fails to recite the finite state machine of the present invention.

In view of the prior comments, Applicants respectfully submit that the cited Jones reference fails to recite or disclose each element of the present invention. Applicants therefore request that the Examiner withdraw the Anticipation rejection to pending claim 1. Applicants additionally request passage of Independent claims 16, 19 and 20-27 to allowance as these claims each contain similar elements to those of claim 1, each of which is not recited by the Jones reference. Furthermore, Applicants submit that dependent claims 2-12, 15, 17, 18 and 28-33 are in condition for allowance, as these claims depend on and further limit that which is claimed in the corresponding independent claims. Applicants therefore urge the Examiner to pass these claims to allowance.

Regarding claims 13 and 14, Applicants submit that in view of the arguments set forth prior claims 13 and 14 are allowable as drafted.

Applicant believes $ 120.00 is due with this statement and herewith requests a one month extension of time. However, if an additional fee is due, please charge our Deposit Account No. 12-0080, under Order No. MWS-069RCE from which the undersigned is authorized to draw.

Dated: July 15, 2005

Respectfully submitted,

By _____

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